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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,708	01/28/2002	Kay Hellig	1458.TT4978	7368

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EXAMINER	
LEBENTRITT, MICHAEL	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,708	HELLIG ET AL.	
	Examiner	Art Unit	
	Michael S. Lebentritt	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004*. and response 8/23/04 rec 8/31/04

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 18-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18 and 33* is/are allowed.

6)☐ Claim(s) *1-7,9-13,19-25 and 27-32* is/are rejected.

7)☒ Claim(s) *8 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Note: Advisory Action mailed on 8/12/2004 is being withdrawn as being premature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,7,19,25 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Long et al, US Patent 6,153,534.

Long discloses forming a gate structure (214) on a substrate (204); forming a dielectric spacer layer (250) over the semiconductor substrate; and etching said dielectric spacer layer without the use of a sacrificial forming spacer, to from L-shape spacers. (figure 7a). Further wherein etching said dielectric spacer layer includes anisotropically etching said dielectric spacer layer to form L- shaped spacers, said L-shaped spacers having vertical portions varying in thickness and horizontal portions varying in thickness. In regards to claim 19, long disclose providing a substrate (204)

having a gate structure (214) formed thereon; forming a dielectric spacer layer (250) over the semiconductor substrate having an exposed surface portion adjacent the gate structure; and etching said exposed surface portion of the dielectric spacer layer to form L-shaped spacers (Figure 7a). In regards to claim 32, providing a substrate (204) having a gate structure (214) formed thereon, forming a dielectric spacer layer (250) over the semiconductor substrate; and etching said dielectric spacer layer, prior to forming any layer overlying the dielectric layer, to form L-shaped spacers. Please see discussion on column 5, line 25 to 6, line 25.

Claims 1,7,19,25,and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Xiang et al, US Patent 6,200,863.

Xiang discloses forming a gate structure (20) on a substrate (16); forming a dielectric spacer layer (24) over the semiconductor substrate; and etching said dielectric spacer layer without the use of a sacrificial forming spacer, to from L-shape spacers. (figure 4). Further wherein etching said dielectric spacer layer includes anisotropically etching said dielectric spacer layer to form L- shaped spacers, said L-shaped spacers having vertical portions varying in thickness and horizontal portions varying in thickness. In regards to claim 19, long disclose providing a substrate (16) having a gate structure (20) formed thereon; forming a dielectric spacer layer (24) over the semiconductor substrate having an exposed surface portion adjacent the gate structure; and etching said exposed surface portion of the dielectric spacer layer to form L-shaped spacers (Figure 7a). In regards to claim 32, providing a substrate (16) having a gate structure (20) formed thereon, forming a dielectric spacer layer (24) over the semiconductor

substrate; and etching said dielectric spacer layer, prior to forming any layer overlying the dielectric layer, to form L-shaped spacers. Please see discussion on column 5, line 25 to 6, line 25.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2,3,4,5, and 20,21,22,23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al as applied to claims 1,7,19,25,and 32 above, and further in view of Haskell, US Patent 4,818,714.

Long is applied supra but lacks the anticipation of forming a liner oxide over said gate structure and wherein said dielectric spacer layer comprises a nitride layer. Long teaches forming an Anti Reflective Coating (ARC) comprising silicon oxynitride (216) over said gate structure (214) and forming a spacer dielectric comprising silicon oxide. Haskell disclose forming a spacer dielectric layer comprising silicon nitride (60) over a liner oxide (50) on said gate structure (30). See figure 4 and 5 and discussion on column 8, line 40 to line 62. In regards to thickness ranges, these values would be optimized through routine experimentation and would not lend themselves to patentability in the instant application, without displaying unexpected results. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of invention to form a liner oxide and dielectric spacer layer, wherein said dielectric spacer

layer comprises a nitride layer as taught by Haskell, in view of the primary reference of Long, because the liner oxide and dielectric spacer layer provide an excellent conformal passivation layer for said gate structure.

Claims 2,3,4,5, and 20,21,22,23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang et al as applied to claims 1,7,19,25,and 32, above, and further in view of Haskell, US Patent 4,818,714.

Xiang is applied supra but lacks the anticipation of forming a liner oxide over said gate structure and wherein said dielectric spacer layer comprises a nitride layer. Xiang teaches forming an Anti Reflective Coating (ARC) comprising silicon oxynitride (22) over said gate structure (20) and forming a spacer dielectric comprising silicon oxide. Haskell disclose forming a spacer dielectric layer comprising silicon nitride (60) over a liner oxide (50) on said gate structure (30). See figure 4 and 5 and discussion on column 8, line 40 to line 62. In regards to thickness ranges, these values would be optimized through routine experimentation and would not lend themselves to patentability in the instant application, without displaying unexpected results. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of invention to form a liner oxide and dielectric spacer layer, wherein said dielectric spacer layer comprises a nitride layer as taught by Haskell, in view of the primary reference of Xiang, because the liner oxide and dielectric spacer layer provide an excellent conformal passivation layer for said gate structure.

Claims 9-13 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al as applied to claims 1,7,19,25,and 32 above, and further in view of Nishizawa, US Patent 6,613,686.

Long is applied supra but lacks the anticipation of etching said dielectric spacer layer with a chemistry combination of CH3F and O2 with an inert gas. Nishizawa teaches etching silicon nitride using CH3F and O2 with an inert gas. In regards to parameter ranges, these values would be optimized through routine experimentation and would not lend themselves to patentability in the instant application, without displaying unexpected results. See figures 2 and 4 and discussion on column 6, line 30 to column 7, line 50. In view of this disclosure it would have been obvious to one or ordinary skill in the art at the time of invention to etch said dielectric spacer layer using an etch chemistry of CH3F and O2 with an inert gas as taught by Nishizawa, in view of the primary reference of Long, because the etch chemistry provides an excellent selectivity ratio for silicon nitride.

Claims 9-13 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang et al as applied to claims 1,7,19,25,and 32 above, and further in view of Nishizawa, US Patent 6,613,686.

Xiang is applied supra but lacks the anticipation of etching said dielectric spacer layer with a chemistry combination of CH3F and O2 with an inert gas. Nishizawa teaches etching silicon nitride using CH3F and O2 with an inert gas. See figures 2 and 4 and discussion on column 6, line 30 to column 7, line 50. In regards to parameter ranges, these values would be optimized through routine experimentation and would not

lend themselves to patentability in the instant application, without displaying unexpected results. In view of this disclosure it would have been obvious to one or ordinary skill in the art at the time of invention to etch said dielectric spacer layer using an etch chemistry of CH3F and O2 with an inert gas as taught by Nishizawa, in view of the primary reference of Xiang, because the etch chemistry provides an excellent selectivity ratio for silicon nitride.

Claims 6 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al as applied to claims 1,7,19,25,and 32 above, and further in view of Verma, US Patent 5,716,880.

Long is applied supra but lacks the anticipation of wherein said dielectric spacer layer comprises a silicon oxynitride layer. Verma discloses wherein spacers (24a-g) made be made from a variety of materials including silicon oxide, silicon nitride and silicon oxynitride. See column 9, line 35 to 65. In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time of invention to from said spacer dielectric comprising silicon oxynitride as taught by Verma, in view of the primary reference of Long, because the spacer dielectric materials silicon oxide, silicon nitride and silicon oxynitride are interchangeably used in semiconductor fabrication.

Claims 6 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang et al as applied to claims 1,7,19,25,and 32 above, and further in view of Verma, US Patent 5,716,880.

Xiang is applied supra but lacks the anticipation of wherein said dielectric spacer

layer comprises a silicon oxynitride layer. Verma discloses wherein spacers (24a-g) made be made from a variety of materials including silicon oxide, silicon nitride and silicon oxynitride. See column 9, line 35 to 65. In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time of invention to from said spacer dielectric comprising silicon oxynitride as taught by Verma, in view of the primary reference of Xiang, because the spacer dielectric materials silicon oxide, silicon nitride and silicon oxynitride are interchangeably used in semiconductor fabrication.

Allowable Subject Matter

Claims 8 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 18 and 33 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: prior art references fail to teach layer to form L-shaped spacers, said L-shaped spacers having vertical portions and a horizontal portion, wherein the horizontal portion varies gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthest from the vertical- portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.

Response to Arguments

Applicant's arguments filed 7/29/04 have been fully considered but they are not persuasive. Applicant argues that neither Long nor Xiang disclose a first and second L-shaped spacer as recited in claim 1: specifically the L- shaped spacers including a first L-shaped spacer immediately adjacent to a first side- wall of the gate structure and a second L-shaped spacer immediately adjacent to a second sidewall of the gate structure. In response to this argument, the courts have held that "although the reference did not disclose a plurality of ribs, the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced"; see in Re Harza. Both Long and Xiang disclose forming a gate structure (214) on a substrate (204); forming a dielectric spacer layer (250) over the semiconductor substrate; and etching said dielectric spacer layer without the use of a sacrificial forming spacer, to from L-shape spacer.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael S. Lebentritt whose telephone number is 571-272-1873. The examiner can normally be reached on 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael S. Lebentritt
Primary Examiner
Art Unit 2824